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F-6810

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Applicant** 

Kenji SHIGEKI, et al.

Serial No.

09/772,027

Filed

January 29, 2001

For

LOGIC INTEGRATED CIRCUIT, AND RECORDING MEDIUM READABLE BY A

COMPUTER, WHICH STORES A SOURCE OF CPU CORE ON SAID LOGIC INTEGRATED

**CIRCUIT** 

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Group Art Unit

**UNKNOWN** 

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INFORMATION DISCLOSURE STATEMENT

Sir:

Submitted herewith is an Information Disclosure Citation together with copies of the documents referred to therein. The degree of relevance of the documents referred to in the Information Disclosure Citation is set forth in the Partial European Search Report also submitted herewith.

I hereby certify that each item of information contained in the Information Disclosure Citation was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement.

Respectfully submitted,

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By

C. Bruce Hamburg Reg. No. 22,389

Attorney for Applicants

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(Rev. 7-80) 42-44F (F-49		Patent and Trademark Office	Applicant: Kenji SHIGEKI, et al.					
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	OTHER INFORMATION E	DISCLOSURE CITA	TIONS (Including	g Author, Title, Date, P	ertinent P	ages, Etc.)		
	9/28/1993 A High WESCON/'93. Co	-Speed RISC C	CPU Using th	ne QL16x24 FPGA		Kleinman	et al.	